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09/632,759	08/04/2000	Richard J. Selvaggi	ATI-000118BN	2358

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EXAMINER	
AMINI, JAVID A	
ART UNIT	**PAPER NUMBER**
2672	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,759	SELVAGGI ET AL.	
	Examiner	Art Unit	
	Javid A Amini	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 17, 2003 has been entered.

Response to Remarks on page 9-14

- Response to remarks on page 11, lines 5-6: Applicant discloses that Ashburn does not filter the image data by the basic state operation to be performed on the data. Examiner's reply: The general definition of filter is: A program or set of features within a program that reads its standard or designated input, transforms the input in some desired way, and then writes the output to its standard or designated output destination (see Microsoft Computer Dictionary fifth edition, page 213). Ashburn in Fig. 4 illustrates the filtering technique. And also see Fig. 14 step 234 sorted edges same as vertices. Ashburn in Fig. 14 illustrates, step 222 number of gates which operations involved the basic state operations. Applicant fails to disclose the novelty and the limitations of the basic state operations. Applicant should specify how many cycles the data required to go through the basic state operations and do the basic state operations (Figs. 3a, 4a, and 5a) combine to each other in order to complete a task?
- Applicant on page 11, lines 14-16 discloses that Ashburn filters the triangle vertex. Examiner's reply: Applicant's claim invention discloses broad languages "image data" or

"image data grouping", and the triangle vertex of Ashburn considers as a image data and number of triangles consider as a image data grouping.

- Applicant on page 12, lines 1-7 discloses that Ashburn apparatus only performs arithmetic operations on data in a particular sequence. If all the equations for the first triangle have not been completed, it would not be possible to achieve the efficiencies desired by this apparatus. Examiner's reply: The correct paragraph from Ashburn on cols. 15-16, lines 65-67; 1-9 is following: the plane equation generation for the second triangle may be performed using results from the plane equation for the first triangle to improve processing efficiency .
- Applicant on page 13, lines 1-5 discloses a term/ a claim language of "a single arithmetic" and referred Examiner to Figs. 3a, 4a and 5a, without defining the limitations/conditions of the term "a single arithmetic"!
- Response to remarks on page 13, lines 17-22 Applicant discloses that most of the triangle plane equations described in Ashburn contain more that one arithmetic operation, as opposed to the present invention. Examiner's reply: the definition of arithmetic is pertaining to the mathematical operations of addition, subtraction, multiplication, and division. The triangle plane has three sides and three vertices; the arithmetic operation computes each parameter of the triangle plane (sides and vertices are equivalent to data image). The combination of these arithmetic operations for three sides and three vertices consider more than one arithmetic operation.
- The rejection of office action still maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-6, 7-9, 11-12, 13-15, and 17-18 rejected under 35 U.S.C. 102(b) as being anticipated by Ashburn U.S. patent 5,651,106, dated July 22, 1997.

1. Claim 1.

A method for processing video image data including a plurality of different image data types, the method comprising the steps of: providing a set of tasks to be performed on each different image data type, each task including one or more basic state operation, each basic state operation being a single arithmetic operation; Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1. Ashburn in Fig. 11 shows the basic state operations under calculate column. **Dividing the image data into a plurality of groups based on the image data type, filtering the basic state operations from all of the image data groups based on the arithmetic operation type;** Ashburn on col. 9, lines 43-55 discloses that the graphics system divides a quadrilateral (image

data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of filtering in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. **Assigning each basic state operation to one of a plurality of commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit;** Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. **Performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and combining the transformed image data of each group.** Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

2. Claim 2.

"The method of claim 1 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 1.

3. Claim 3.

"The method of claim 1 wherein the plurality of said commonly used arithmetic units includes an addition unit and a multiplication unit". See rejection of claim 1.

4. Claim 5.

"The method of claim 1 further comprising the step of providing a queue for each of the plurality of commonly used arithmetic units wherein each assigned arithmetic operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

5. Claim 6.

"The method of claim 5, wherein the basic state operations of each task can be performed by different arithmetic units, the basic state operations to be performed in a predetermined sequence, the method further comprising the step of preventing the basic state units from performing the arithmetic operations of a task out of sequence". This step is inherent because if

the design of a task is correct, the arithmetic operations will follow the sequence, otherwise the task operates out of sequence.

6. Claim 7.

An apparatus for processing video image data including a plurality of different image data types, the apparatus comprising: means for providing a set of tasks to be performed on each different image data type, each task including one or more basic state operation, each basic state operation being a single arithmetic operation; Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1. Ashburn in Fig. 11 shows the basic state operations under calculate column. **Means for dividing the image data into a plurality of groups based on the image data type; means for filtering the basic state operations from all of the image data groups based on the arithmetic operation type**; Ashburn on col. 9, lines 43-55 discloses that the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of filtering in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. **Means for assigning each basic state operation to one of a plurality of**

commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit; Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. **Means for performing each basic state operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided set of tasks; and mean for combining the transformed image data of each group**;". Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

7. Claim 8.

"The apparatus of claim 7 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 7.

8. Claim 9.

"The apparatus of claim 7 wherein the plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 7.

9. Claim 11.

"The apparatus of claim 7 further comprising a queue for each of said commonly used arithmetic units and wherein each basic state operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

10. Claim 12.

"The apparatus of claim 11, wherein the basic state operations of a task are to be performed in a predetermined sequence, the apparatus further comprising means for preventing the arithmetic units from performing the basic state operation of a task out of sequence". This step is inherent because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

11. Claim 13.

"**An apparatus for performing video processing, the video processing including performing a set of tasks on vertex parameters, the apparatus comprising: a scheduler having an input configured to receive the set of tasks, said scheduler arranging the vertex parameters to be processed into a plurality of groups based on in part characteristics of the vertex parameters;** Ashburn on col. 8, lines 63-67, and also see Fig. 2, discloses that In an alternative embodiment, both the left and right stacks contain identical hardware, including

dividers. In this configuration, functionality may be partitioned such that each stack performs the same operations on different primitives. Applicant does not explicitly specify the definition of claim language of a single arithmetic operation and basic state operations; therefore, Ashburn in Fig. 6 illustrates a single arithmetic operation for edge 1. Ashburn in Fig. 11 shows the basic state operations under calculate column. **A sequencer for each group, said sequencer: selecting the tasks required to process that group's parameters**; Ashburn on col. 6, lines 36-41 discloses that unlike conventional texture mapping systems that download the entire series (sequence) of MIP maps for any primitive being rendered, the present invention downloads only the portion of the series of MIP maps actually needed to currently render the primitive or the currently rendered portion thereof.. **Determining a set of basic state operations required to accomplish that group's tasks, wherein each basic state operation is a single arithmetic operation; filtering the basic state operations from all of the image data groups based on the arithmetic operation type;** Ashburn on col. 9, lines 43-55 discloses that the graphics system divides a quadrilateral (image data) into two triangles (groups) so that the plane equation generation for the second triangle may be performed more efficiently by using results from the plane equation generation for the first triangle. Applicant does not specify the type of filtering in the claim invention therefore, Ashburn on col. 12, lines 32-38 discloses that the vertices are typically sorted (filter) so that edge1 is always the long (in Y) edge as shown in Figs. 5a and 5b. **Assigning each basic state operation to be performed to one of a plurality of commonly used arithmetic units based on the corresponding arithmetic operation type, wherein all basic state operations of the same arithmetic operation type are assigned to the same arithmetic unit;** Ashburn in Figs. 2 and 3 illustrates ALU 184 performs arithmetic operations

such as additions and subtractions (considered to be basic state operations that are assigned to 184), while multiplier 186 and divider 188 (considered to be basic state operations) respectively perform multiplies and divides. **And sending each of the basic state operations of each of that group's tasks to the arithmetic unit associated with that basic state operation; and each of said commonly used arithmetic units, having an input configured to receive the sent basic state operations and vertex parameters associated with the sent operations, each arithmetic unit performing the sent basic state operations on the sent vertex parameters**; Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R, G, B color control signals for each pixel are respectively provided over R, G, B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

12. Claim 14.

"The apparatus of claim 13 wherein the plurality of groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". Ashburn illustrates in Fig. 1A that the distributor chip 30 receives the X,Y,Z coordinate and color primitive data over bus 16 from the host computer, and distributes 3-D primitive data evenly among the 3-D geometry accelerator chips 32A, 32B and 32C. The texture mapping data transfers over bus 94. In this manner, the system bandwidth is increased because three groups of primitives are operated upon simultaneously.

13. Claim 15.

"The apparatus of claim 13 wherein said plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 13.

14. Claim 17.

"The apparatus of claim 13 further comprising a queue for each of said commonly used arithmetic units and wherein the sent basic state operations are sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

15. Claim 18.

"The apparatus of claim 17 wherein the basic state operations of a task are to be performed in a predetermined sequence and said sequencer prevents said arithmetic units from performing the basic state operations of a task out of sequence". This step is inherent because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-746-8705.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Javid A Amini
Examiner
Art Unit 2672

Javid Amini

JEFFERY BRIER
PRIMARY EXAMINER